Data Sheet

VIAVI Solutions

VIAVI

Xgig 4-lane Exerciser

for PCI Express® 6.0

This PCIe Exerciser generates PCIe 6.0 data streams and responses for in-depth testing and analysis at 64GT/s.

The VIAVI Xgig® PCIe 6.0 6P4 Exerciser brings the next generation of high-speed test capability to the Xgig PCIe product portfolio. An Exerciser is a valuable tool for debugging difficult protocol communication problems because it provides full, bit-level, repeatable control over PCIe data traffic.

An Exerciser generates and responds to PCIe 6.0 64GT/s traffic. It can be configured to emulate the operation of a Root Complex (RC) or an Endpoint (EP) device, effectively acting as a highly-configurable link partner for testing Hosts and Endpoint Devices. Further, Ordered Sets (TS0, TS1, TS2, etc.), and TLP, DLLP, and LTSSM sequences can be defined, run, and even modified in real-time based on inputs. The 6P4 supports PCIe FLIT Mode and Non FLIT Mode operation.

The 6P4 also supports detailed validation and debug of the state machine of a PCIe 6.0 controller. It enables debug and performance tuning of firmware and application software. The Exerciser can be programmed to non-compliant PCIe sequences to enable testing of boundary and stress conditions that are not normal to correct system operation, and would otherwise be very difficult to evaluate.

The Exerciser has built-in analysis capabilities and is enabled automatically to capture full duplex data between the Exerciser and its link partner. Bidirectional data can be saved for detailed analysis using VIAVI tools such as Expert™.

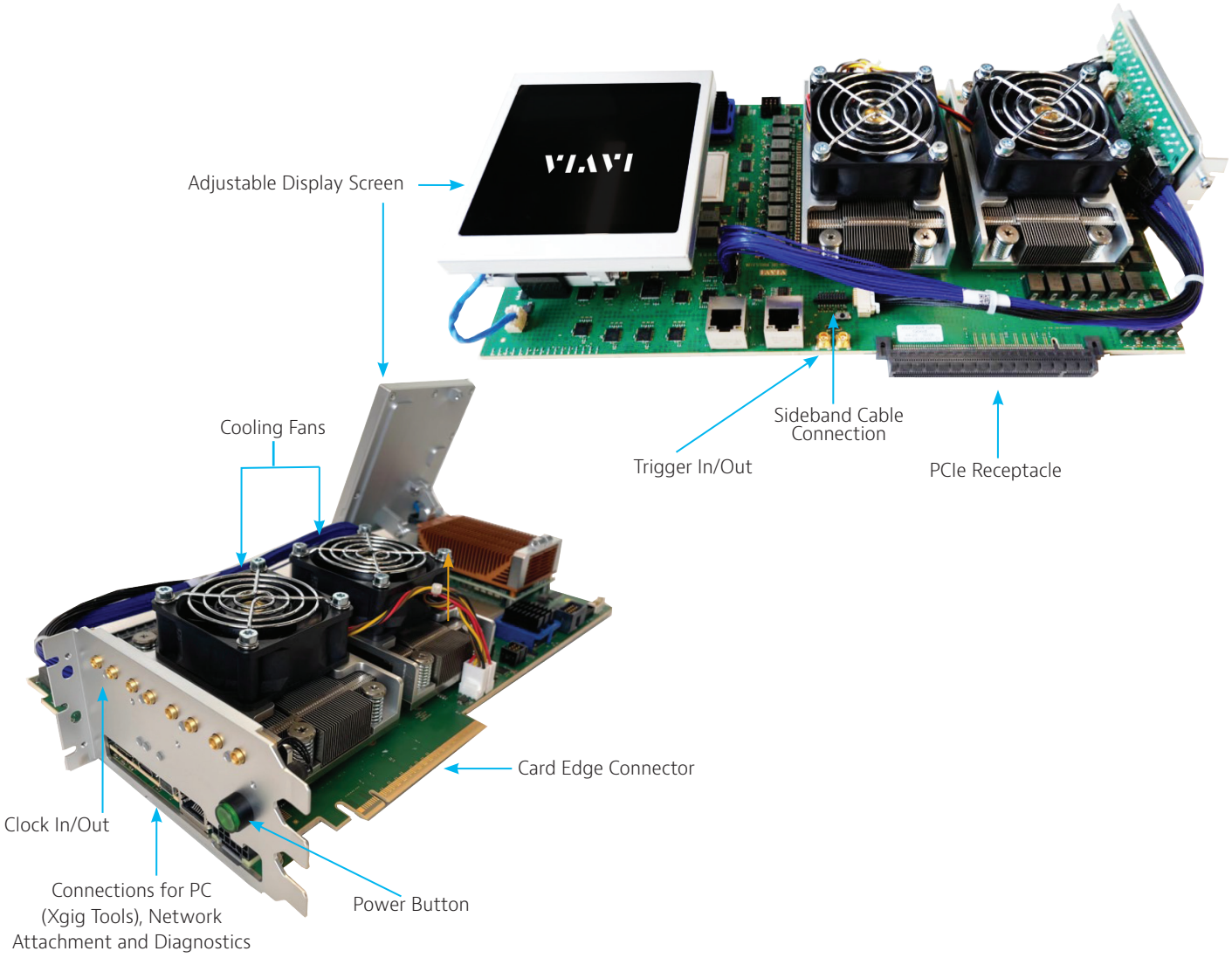
A scripting API is available so that complex, custom Exerciser test scripts can be created; either as original or modified from pre-defined library scripts.

The VIAVI PCIe 6.0 Exerciser is a fully integrated solution with Exerciser functionality provided in a single CEM card form factor.

Key Features

- Allows capture and analysis of traffic flows between the Exerciser and its link partner
- Generates and responds to PCIe 6.0 64GT/s compliant data packets
- Operates to 64GT/s PAM4, and supports all other PCIe data rates of of 2.5, 5.0, 8.0, 16, and 32GT/s NRZ
- Supports links of 1, 2 and 4 lanes
- 32GB total memory (16GB upstream capture and 16GB downstream capture)
- User can set link rates and widths and control transitions to other rates
- Fully integrated Analyzer function enables a variety of test conditions
- Support for new PCIe FLIT Mode, FEC and TS0 Ordered Set
- LTSSM state tracker with history log
- User-configurable custom test configurations for positive and negative test cases
- Scripting API allows creation of complex, user-defined test cases
- Powerful graphical control interface provides quick status information and fast setup of test cases
- Xgig tools and the Exerciser user interface operate on a Windows enabled PC

Xgig 6P4, 4-lane Exerciser for PCIe 6.0



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Xgig Exerciser Interface – Start Page

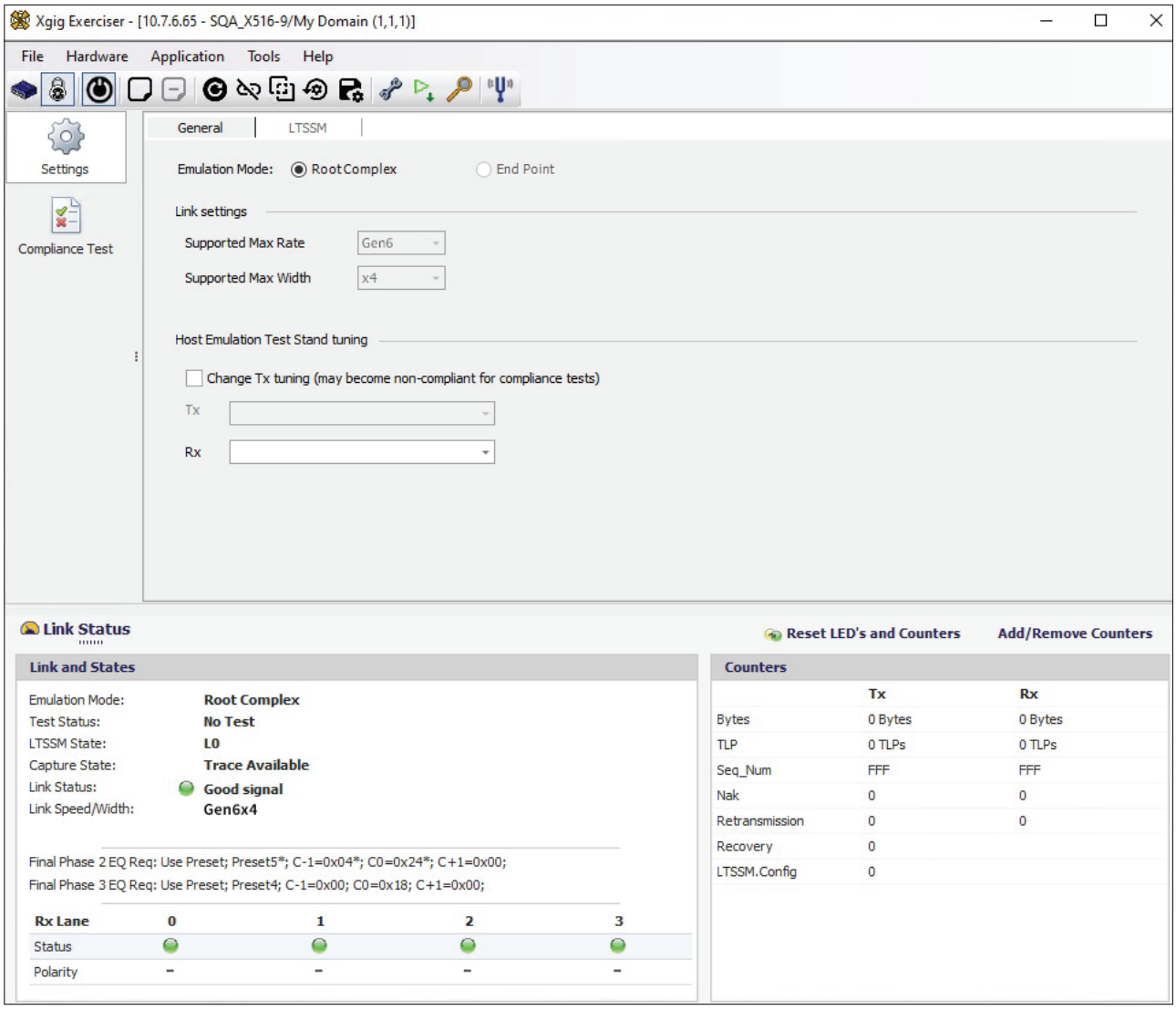

Figure 1 – Exerciser Start Screen

Exerciser User Interface

The Xgig PCIe Exerciser user interface makes it easy to set up and execute a test. Figure 1 above shows the Exerciser launch screen. The top bar includes the typical Windows™ control items. The second bar down has various quick launch buttons for tasks done often.

On the left side are icons for Settings, Compliance Tests, and other features. The Settings>General tab is the first that is presented. Information on the test bench configuration is provided including clocking, reset and other basic controls.

From Settings, controls for the extensive Exerciser parameters are accessible. The LTSSM tab provides control over link settings and operation.

For example, TX and RX setting can be adjusted from this tab. It also allows setting timeouts and other parameters. The Settings tab allows forcing limits on the test data rate and maximum link width.

Below the Settings icon, the Compliance Test icon opens a panel for selecting tests to be run.

Below the Compliance Test icon the Config Space icon opens for defining the Exerciser's PCIe configuration space parameters.

Always available at the bottom of the Exerciser window is the current test and bench status.

Test Applications

The following table lists some of the features available and tests that can be done using the Xgig PCIe Exerciser.

Support for new PCIe FLIT Mode	Define ROM write address space size and offset
Support for new PCIe FEC	Define Cfg read address space size and offset
Support for new TS0 Ordered Set	Define Mem64 read address space size and offset
Support for 64GT/s PCIe 6.0 PAM-4 signaling	Define Mem32 read address space size and offset
Control clock sources	Define IO read address space size and offset
Control and validate reset functions	Define ROM read address space size and offset
Control DUT power	Supports Config Space Type 0 Headers (32b)
LTSSM supported states: Detect, Quiet, Configuration, L0, L1, Recovery	Supports Config Space Type 1 Headers (64b)
Set data rate	Inject disparity errors option
Set link width	Inject symbol errors option
Edit LTSSM state transitions	Inject Sync Bit errors option
Control link width changes	Define ACK/NACK policies
Control link rate changes	Control ACK/NACK DLLP generation/reception
Test transitions: any speed/width to any other	Control idle generation
Control link state changes	Auto generate TLP sequence numbers
Set TX parameters	Auto generate TLP LCRC
Set RX parameters	Auto retransmit TLPs that NACK'd
Control equalization procedure	Validate state timeouts
Generates TLP 32b memory packets	Set replay timeouts
Generates TLP 64b memory packets	Control SKP generation
Generates TLP IO packets	Control over 8b/10b and 128b/130b encoding
Generates TLP configuration packets	Control and monitor sideband signals
Generates TLP message packets	Define custom test configurations, save and load
Execute bad TLP packets	Define custom test suites and execution sequence
Define TS0/TS1/TS2 data	View test description
Define Cfg write address space size and offset	View test results
Define Mem64 write address space size and offset	View LTSSM log
Define Mem32 write address space size and offset	View extensive error count information
Define IO write address space size and offset	

Ordering Information

Part Number	Description
XGIG6P-PCIE6-X4-PF	PCIe 6.0 4-Lane Exerciser Platform
XGIG6P-PCIE6-X4-EX	PCIe 6.0 4-Lane Exerciser License Key

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